

FIG. 1 is a schematic diagram of a system 20 for processing data. The system 20 includes a data source 22, a data processor 24, a data storage 26, a data output 28, and a data interface 30. The data source 22 is connected to the data processor 24, which is connected to the data storage 26. The data processor 24 is also connected to the data output 28. The data interface 30 is connected to the data processor 24 and the data storage 26. The data source 22 is represented by a stack of rectangular blocks 103, 104, and 105. The data processor 24 is represented by a stack of rectangular blocks 106, 107, 108, and 109. The data storage 26 is represented by a cylindrical shape 100. The data output 28 is represented by a rectangular block 28. The data interface 30 is represented by a rectangular block 30. The system 20 is shown in a perspective view. The data source 22 is connected to the data processor 24 by a line 101. The data processor 24 is connected to the data storage 26 by a line 102a, 102b, and 102c. The data processor 24 is also connected to the data output 28 by a line 103. The data interface 30 is connected to the data processor 24 by a line 104. The data interface 30 is also connected to the data storage 26 by a line 105. The data source 22 is connected to the data processor 24 by a line 106. The data processor 24 is connected to the data storage 26 by a line 107. The data processor 24 is also connected to the data output 28 by a line 108. The data interface 30 is connected to the data processor 24 by a line 109. The data interface 30 is also connected to the data storage 26 by a line 110.

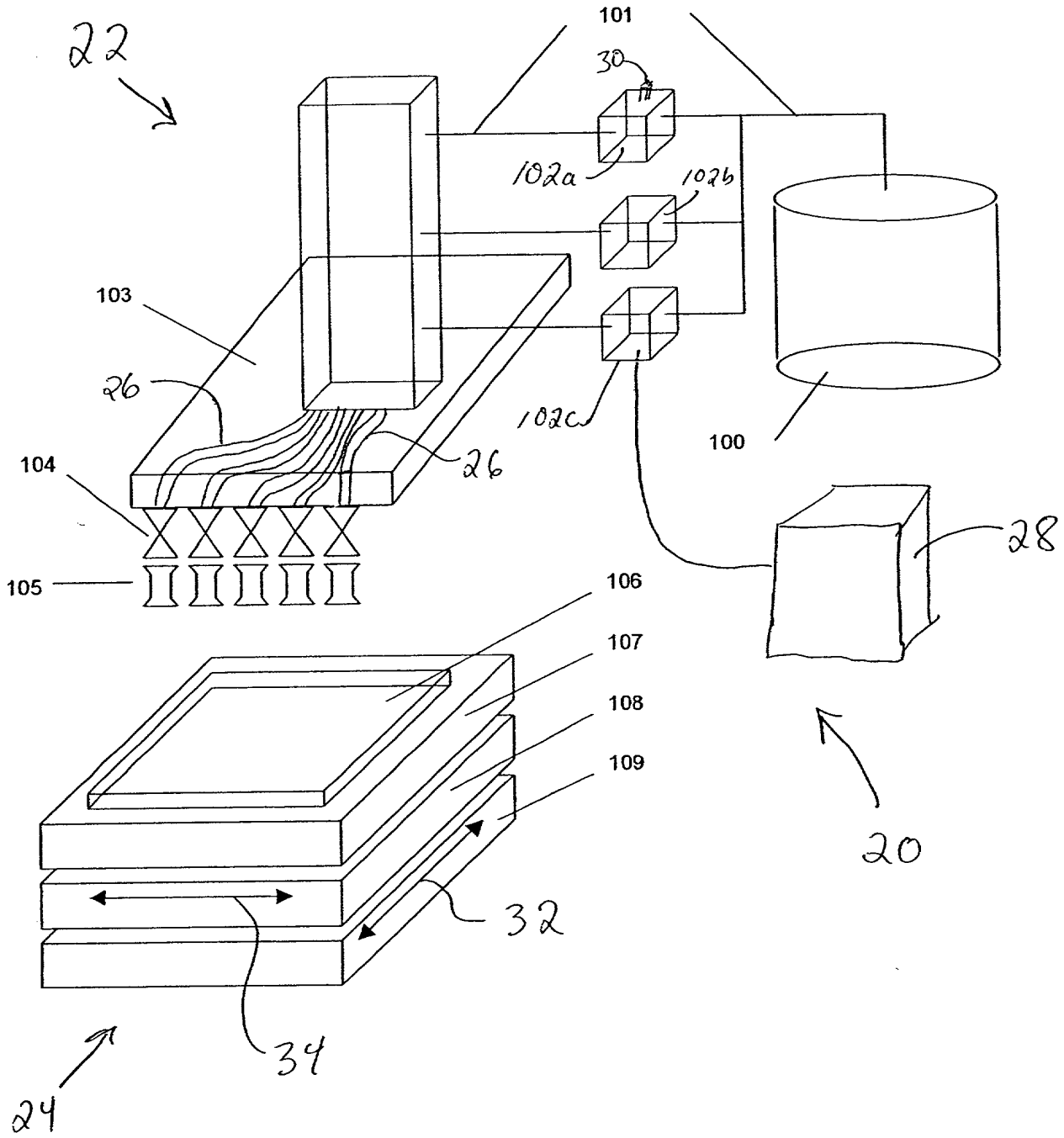


Figure 1

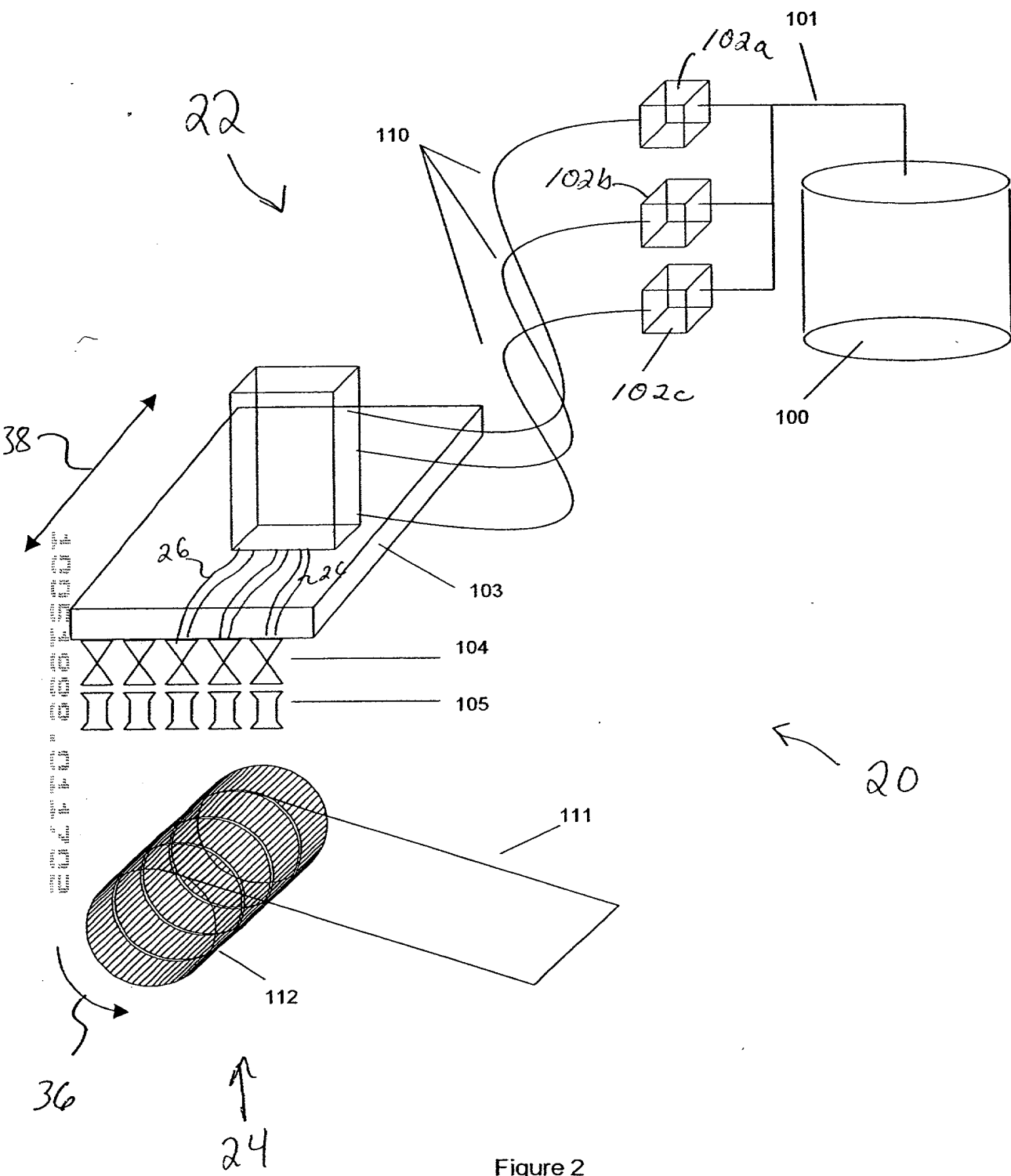


Figure 2

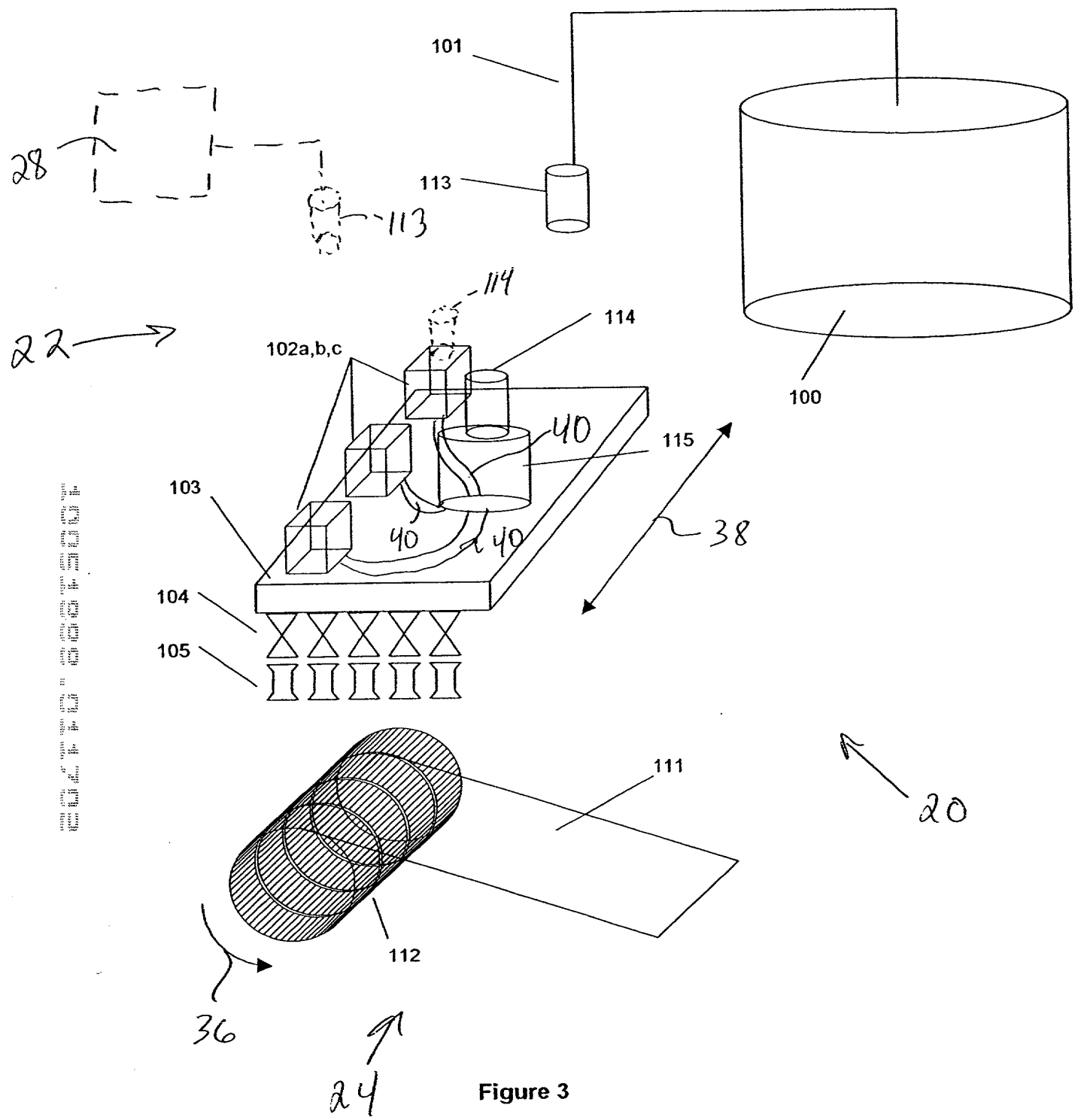


Figure 3

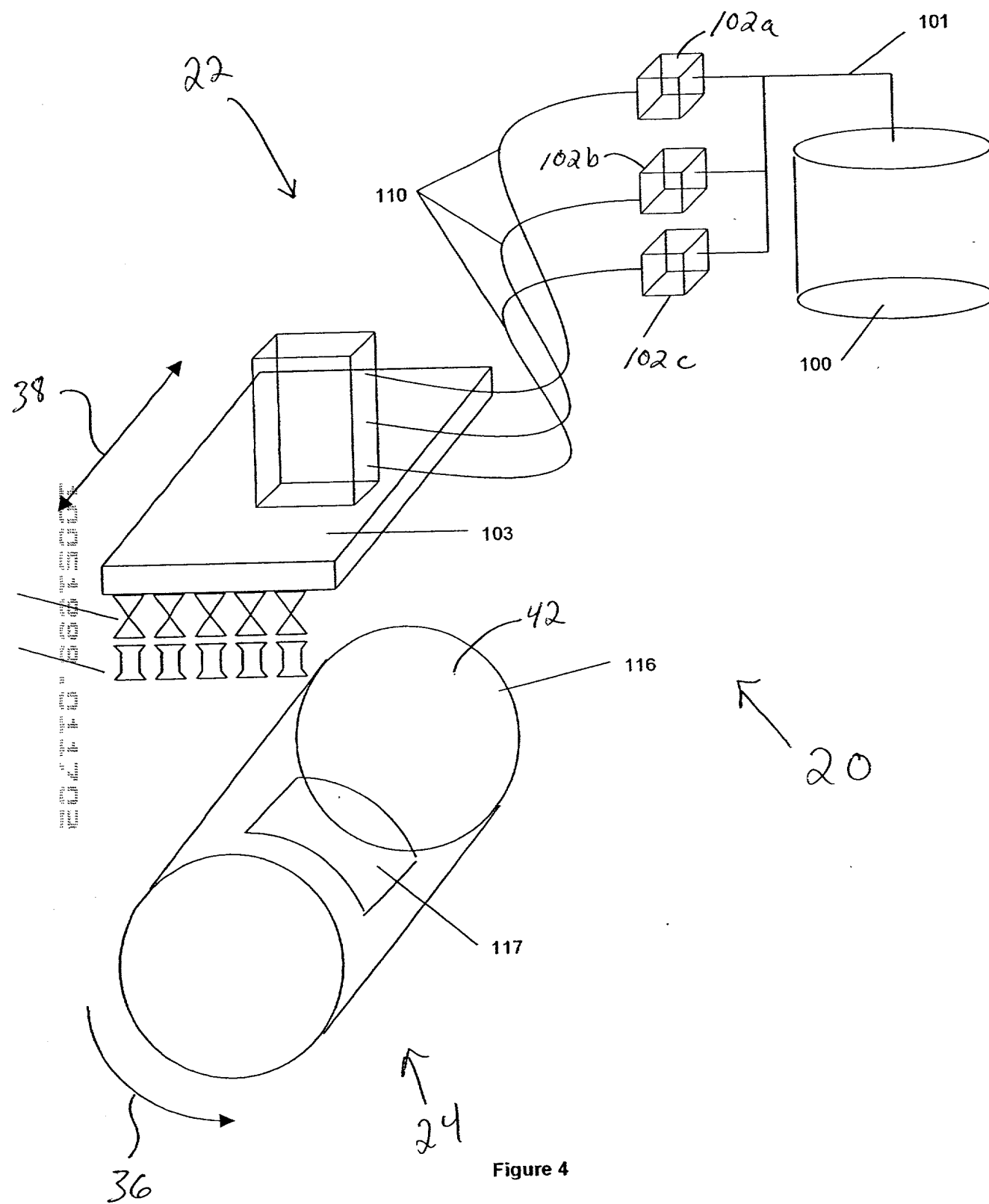


Figure 4

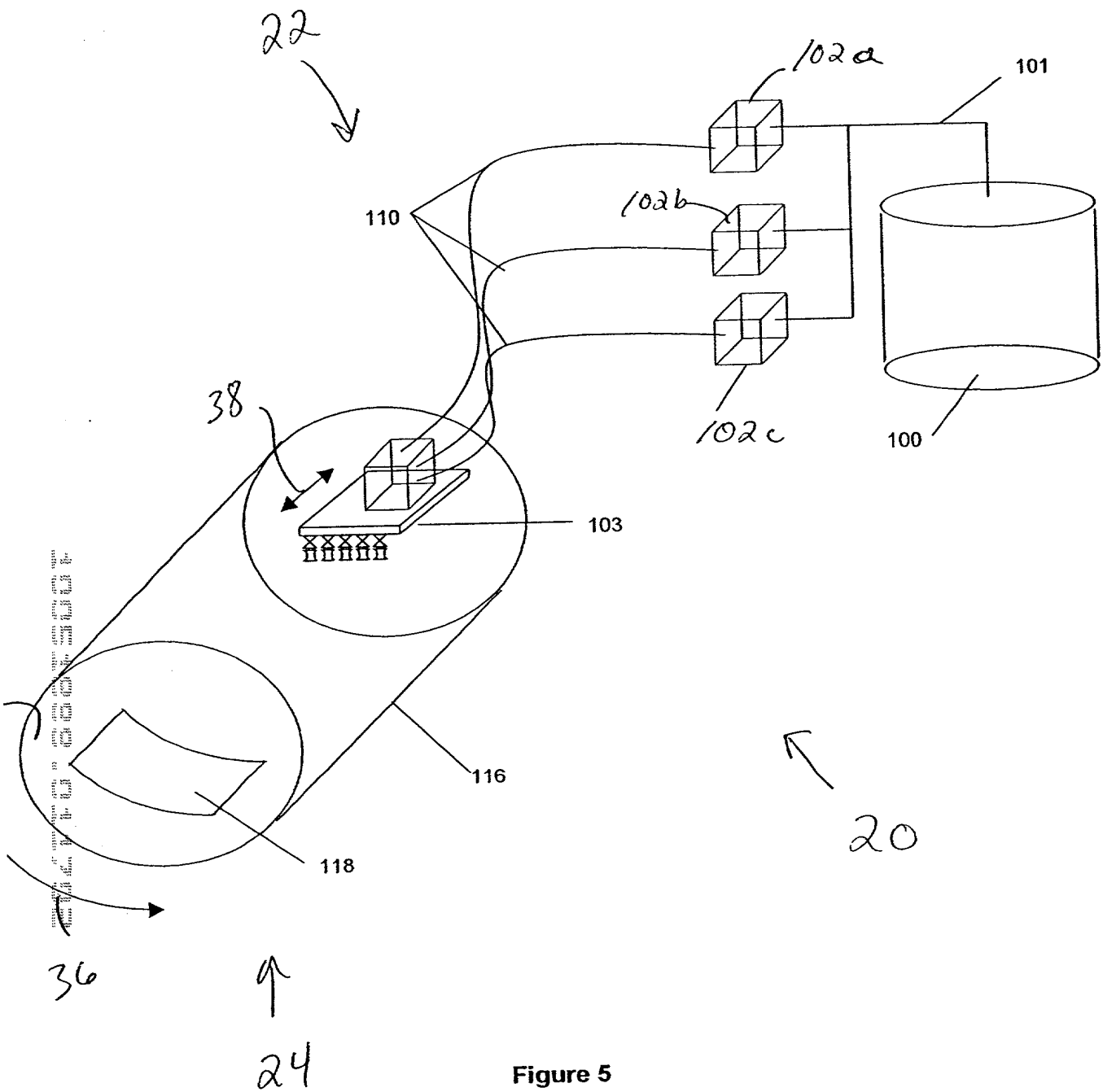


Figure 5

FIG. 6A is a schematic diagram of a device in a first state, and FIG. 6B is a schematic diagram of the device in a second state.

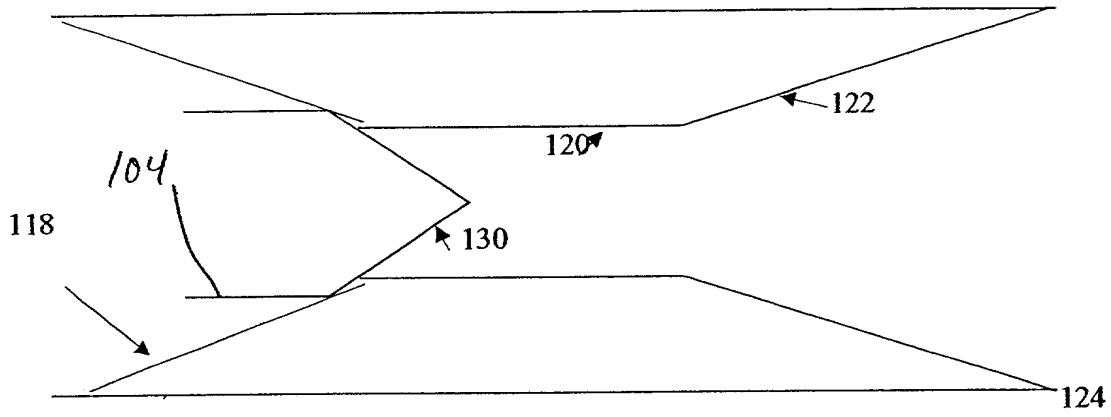


FIG. 6A

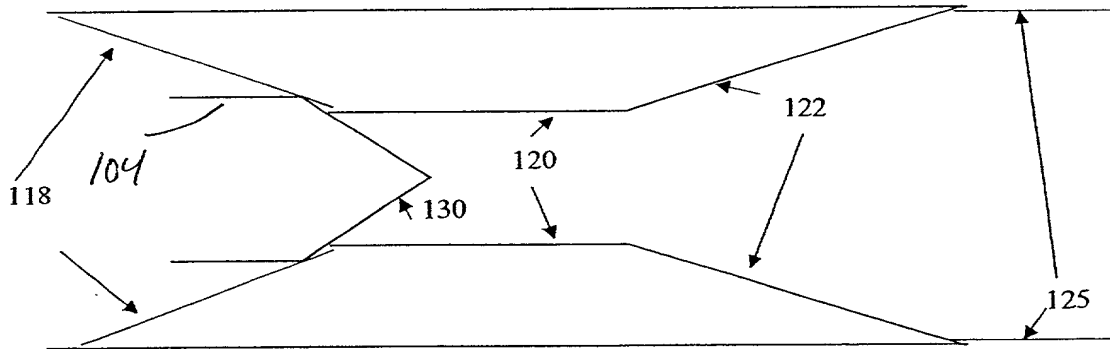


FIG. 6B

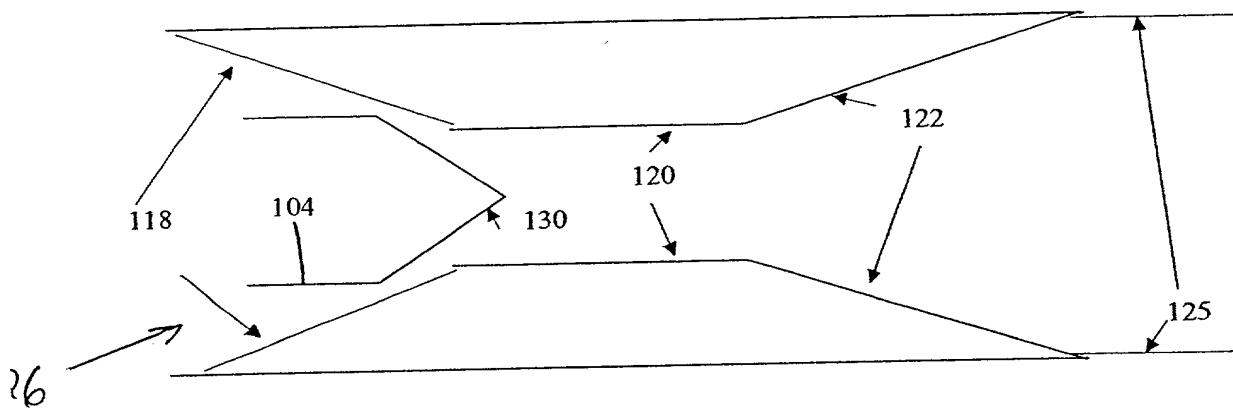


FIG. 7A

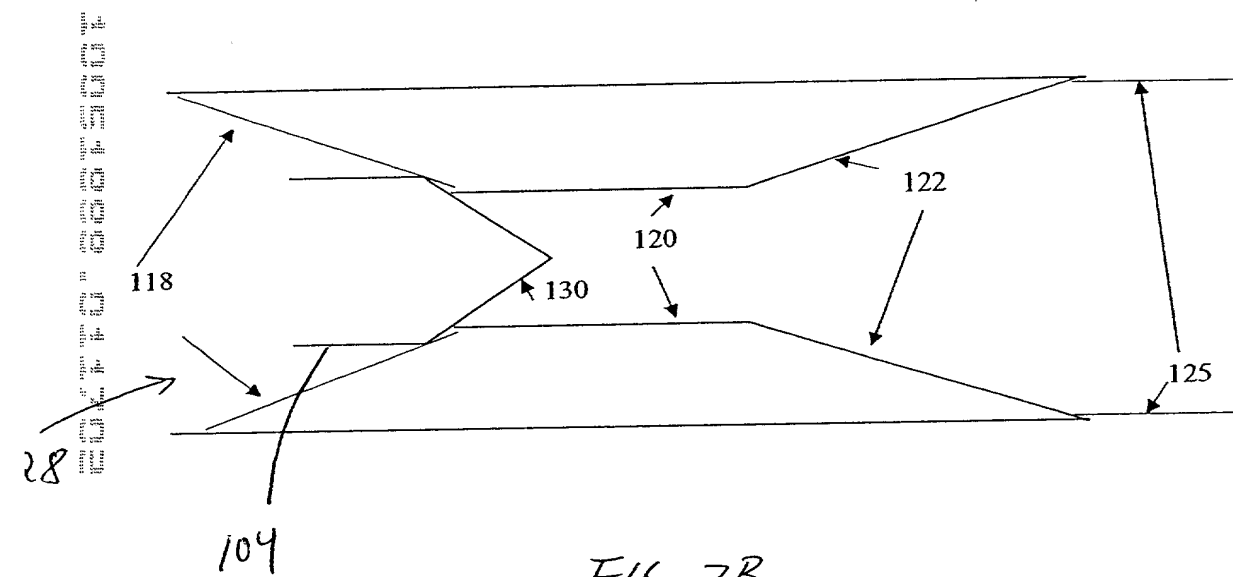


FIG. 7B

FIG. 8 is a perspective view of a device 100 in accordance with one embodiment of the present invention. The device 100 includes a base 101, a top layer 102, a middle layer 103, and a bottom layer 104. The base 101 is formed by a series of vertical pillars 105. The top layer 102 is formed by a series of horizontal pillars 106. The middle layer 103 is formed by a series of horizontal pillars 107. The bottom layer 104 is formed by a series of horizontal pillars 108. The device 100 is shown in a perspective view, with the top layer 102 and middle layer 103 being slightly offset from the base 101 and bottom layer 104. The device 100 is shown in a perspective view, with the top layer 102 and middle layer 103 being slightly offset from the base 101 and bottom layer 104.

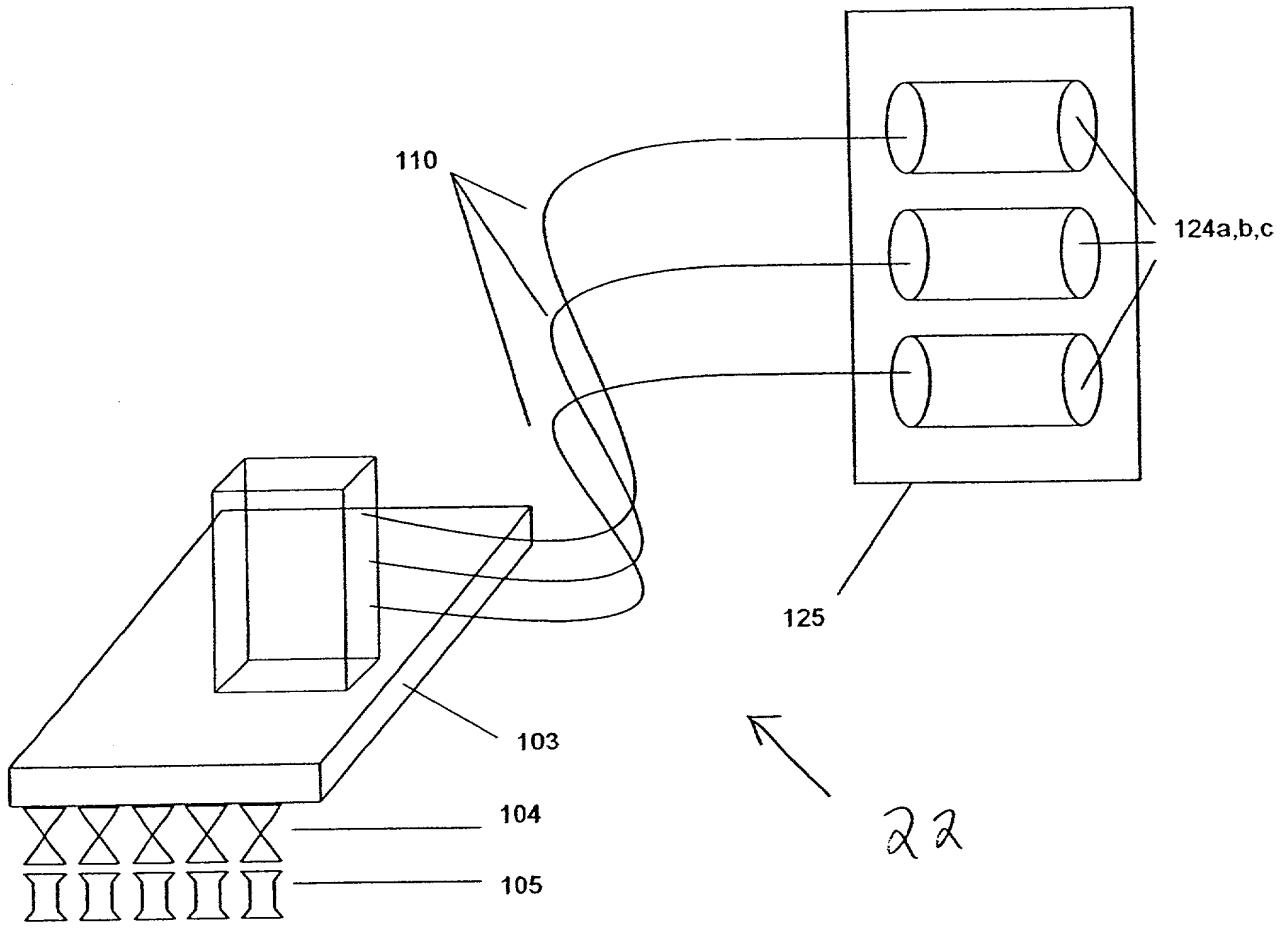


FIG. 8



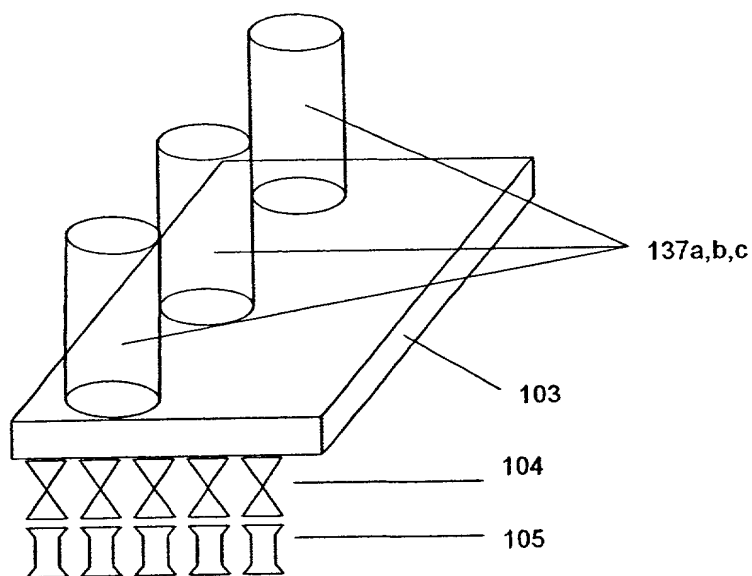


FIG. 9A

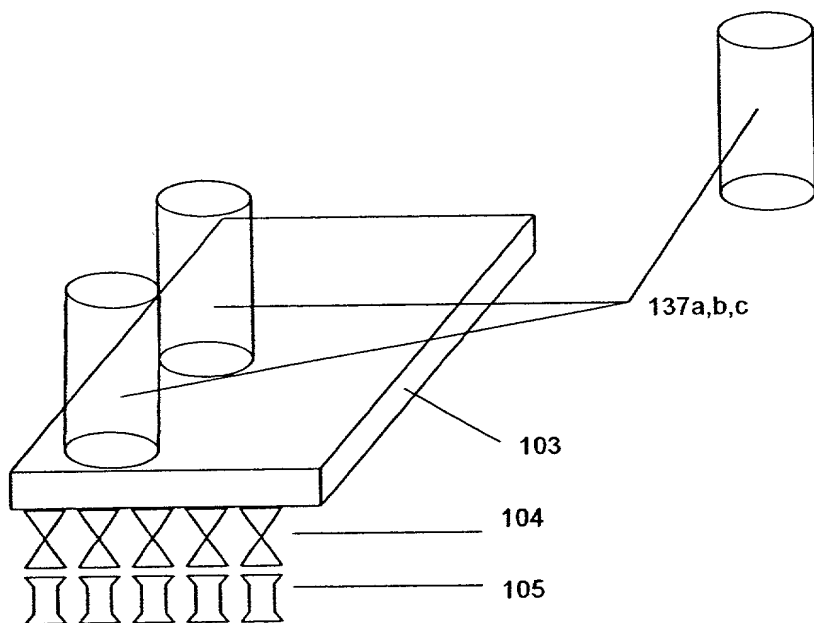


FIG. 9B

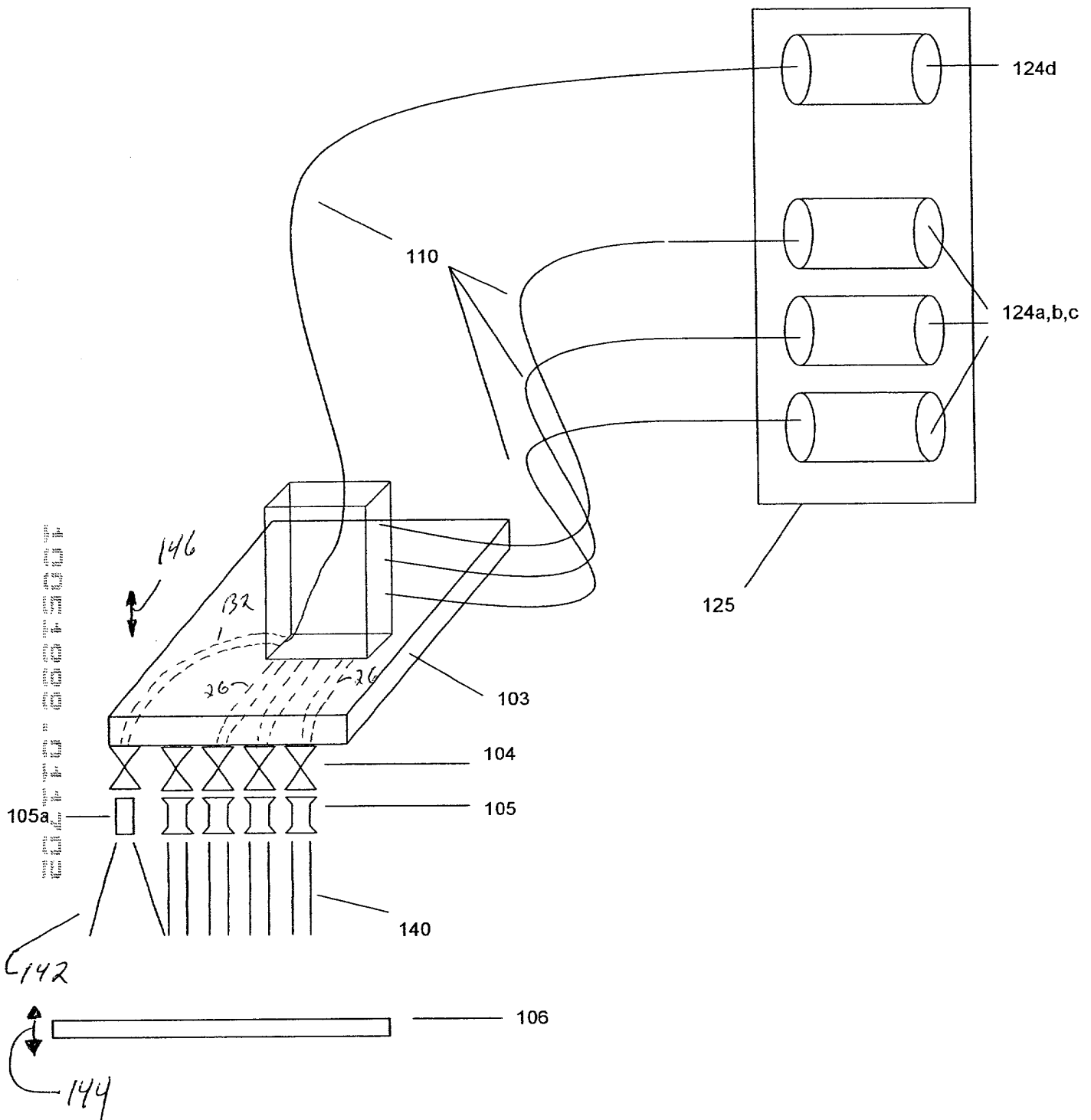


FIG. 10

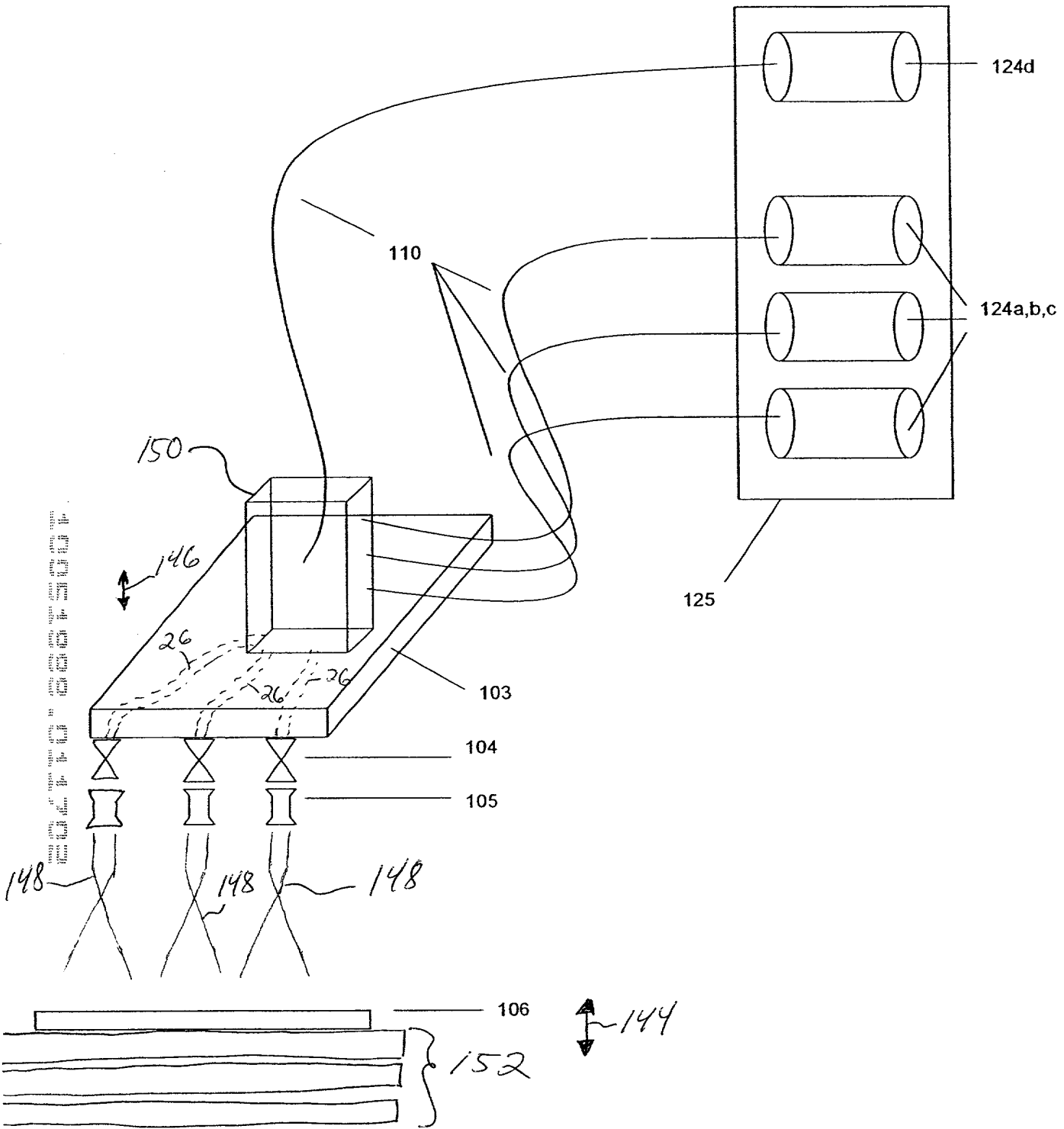


FIG. 11A

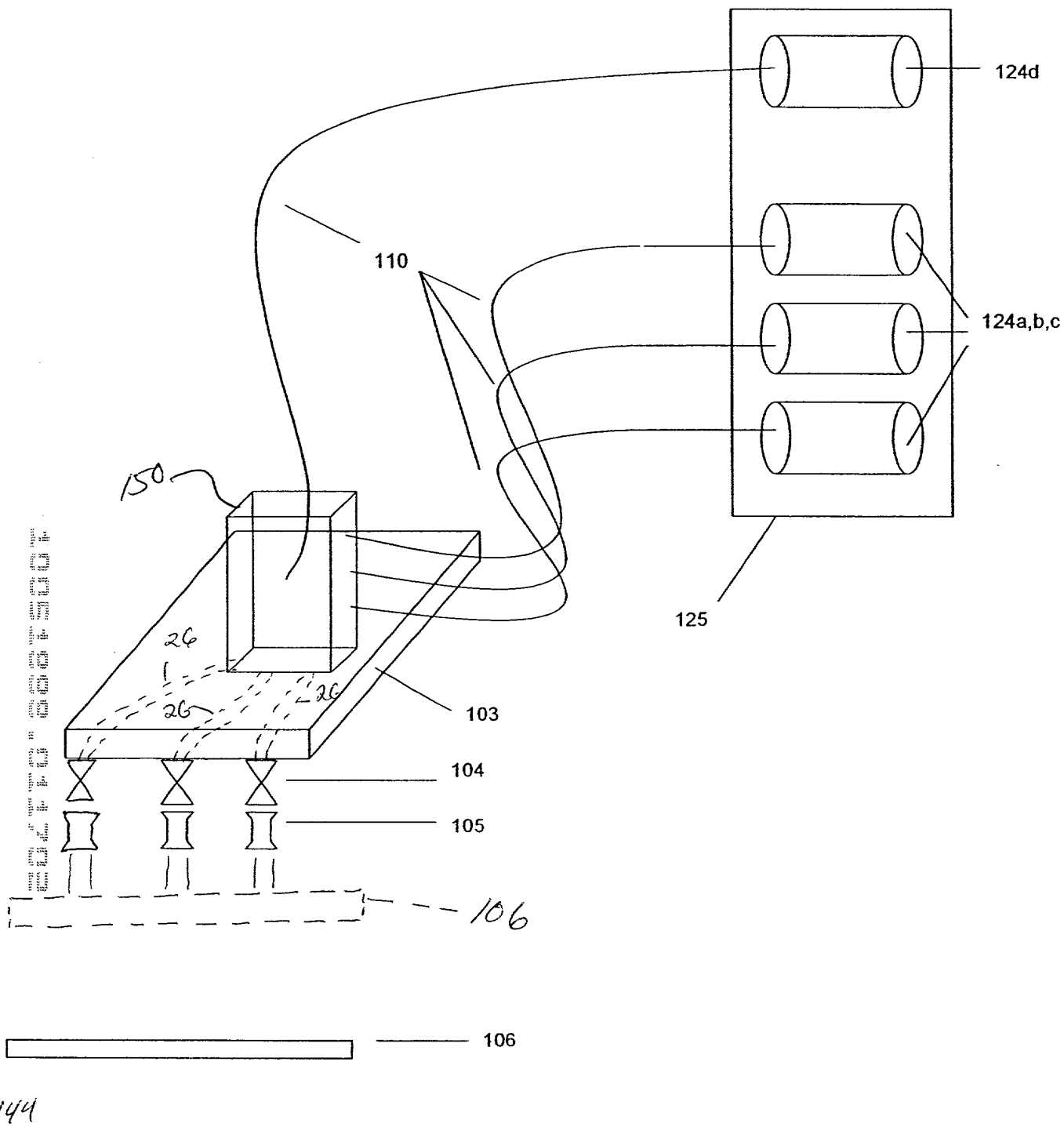


FIG. 11B

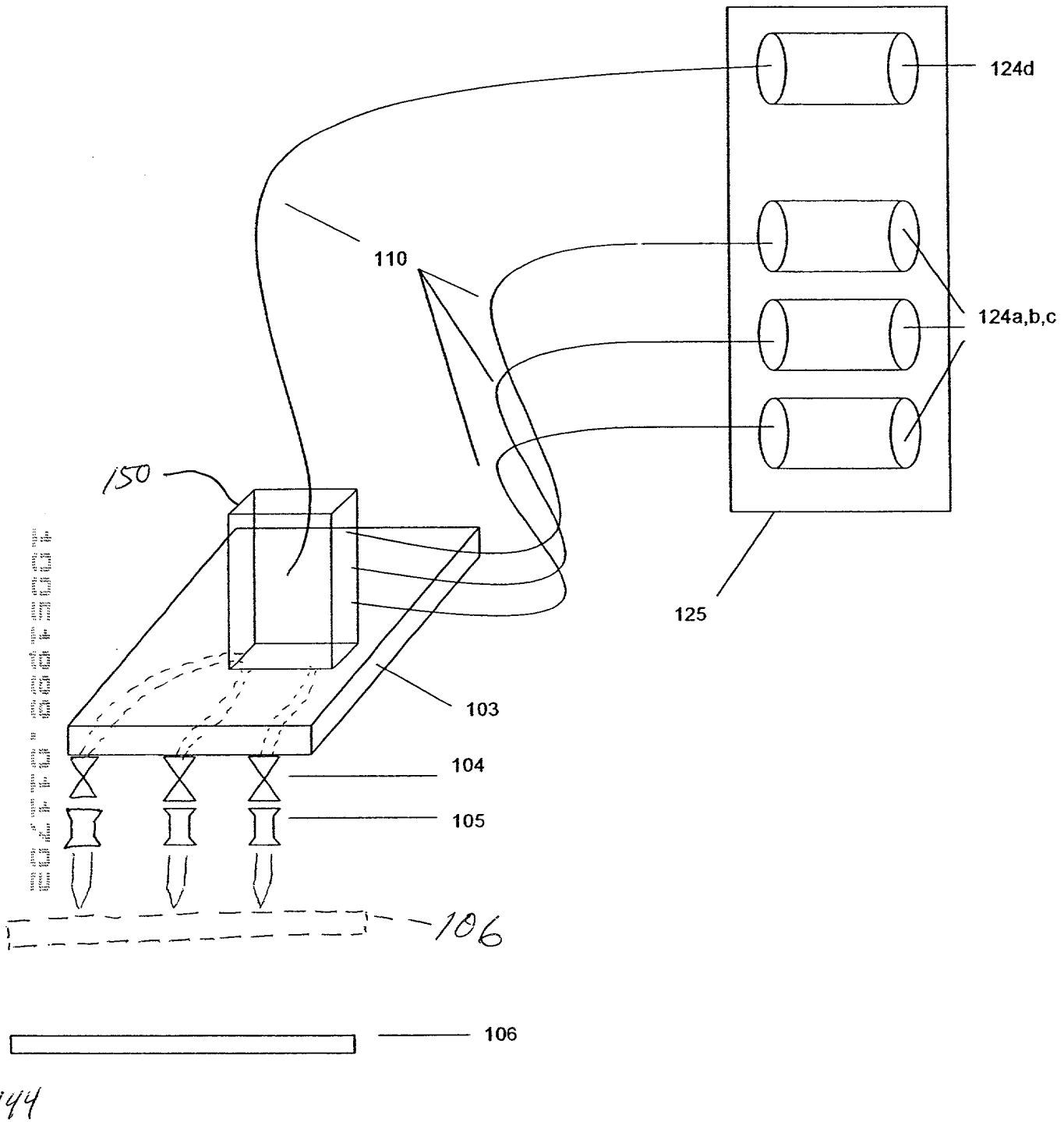


FIG. 11C

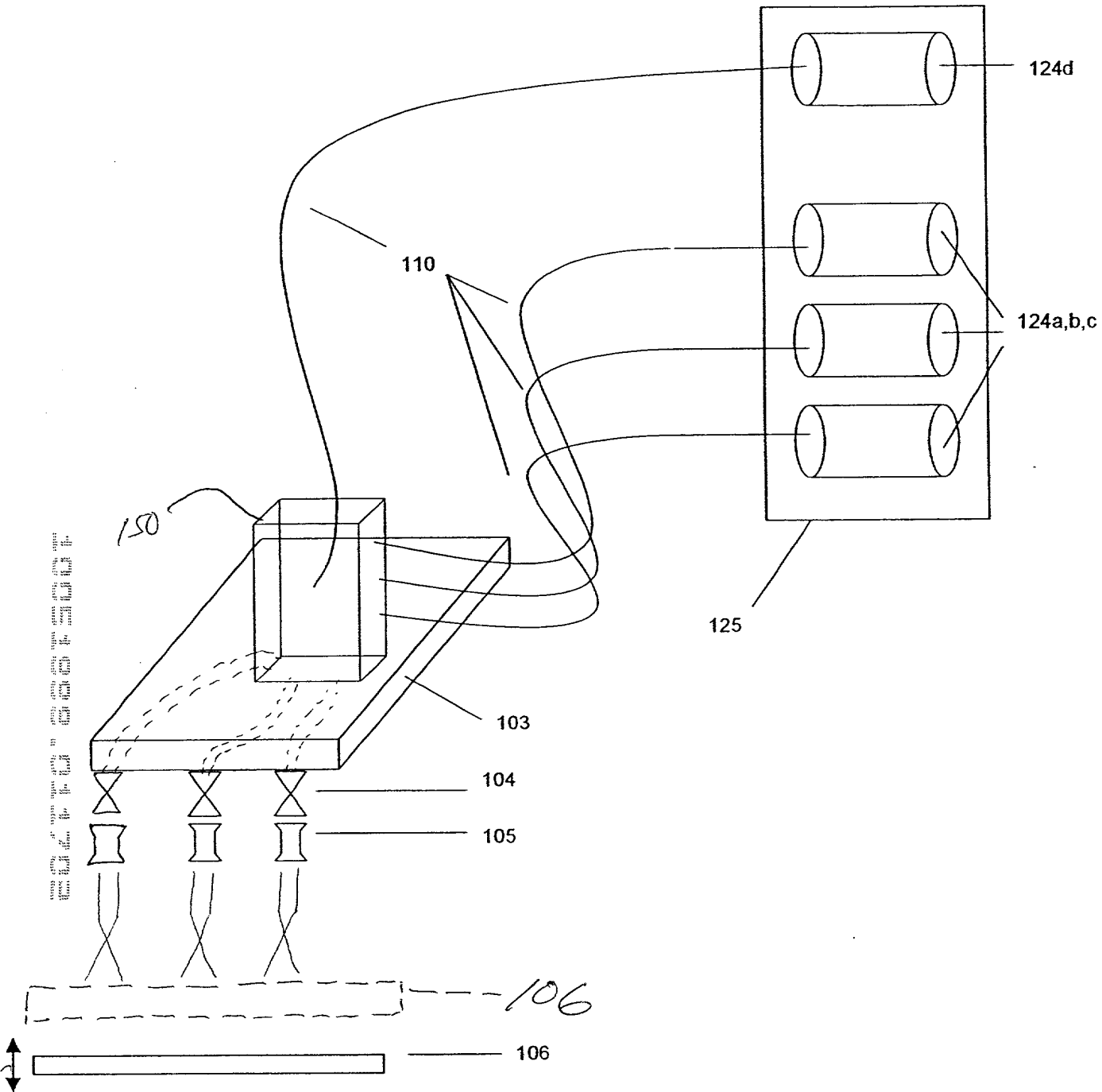


FIG. 11D